RECEIVED
CENTRAL FAX CENTER
SEP 19 2007

Remarks/Arguments:

Claims 1-22 are presently pending. Claims 1-6, 8-12, 14-18, 21, and 22 stand rejected and claims 7, 13, 19, and 20 are identified as objected to. Applicant notes that claim 13 is identified as objected to, but the text of the Office Action sets forth a rejection of claim 13. Accordingly, applicant will treat claim 13 as if it is rejected. Reconsideration of the rejected claims is respectfully requested based on the following remarks.

Section 6 of the Office Action recites "[c]laims 1-6, 8-12, [13,] 14-18, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533) and further in view of Payson (7,193,994)." It is respectfully submitted, however, that these claims are allowable over US Patent Application Publication No. 2004/0088472 to Nystuen (Nystuen), US Patent No. 4,683,533 to Shiozaki et al. (Shiozaki), US Patent No. 7,193,994 to Payson (Payson), and combinations thereof for the reasons set forth below.

Briefly, Nystuen is directed to a multi-mode memory controller for receiving successive memory access requests, Shiozaki is directed to a storage control system using a plurality of buffer address arrays, and Payson is directed to a crossbar synchronization technique. The claims in the instant application are directed to controllers, systems, and methods for managing memory requests from a plurality of requesters.

Claim 1 includes at least one feature that is neither disclosed or suggested by the applied references. Claim 1 includes the following features:

> an arbiter having a plurality of request ports, each request port configured to receive the memory requests from a respective one of the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests;
>
> a first path controller coupled to the arbiter and the plurality of memory banks, the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request for a first data transfer;
>
> a second path controller coupled to the arbiter and the plurality of memory banks, the second path controller configured to process the second memory request in the second processing path to activate,

> during the first data transfer, a second memory bank associated with the second memory request for a second data transfer; and
>
> a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, and the first and second data transfers do not conflict.

This means that an arbiter receives memory requests to access a plurality of memory banks via a plurality of request ports. The arbiter assigns the memory requests received via the request ports to a first processing path and a second processing path taking into account the memory banks requested by the received and assigned memory requests. *See paragraph [0033] and element 112 in Figure 2 of the instant application.*

Nystuen is directed to a memory controller that includes an arbiter connected to a memory device via a single processing path. Specifically, in figure 3, Nystuen teaches a single processing path 334 that the arbiter utilizes to send successive commands and addresses to memory device 302. All memory request are processed through path 334 successively. Accordingly, Nystuen does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths as set forth in claim 1.

Shiozaki is directed to a storage control system that includes two controllers that direct successive memory requests over a single processing path. Specifically, in figure 1, Shiozaki teaches a single processing path 14 that a storage control unit 2 utilizes to send successive memory requests to main storage 3. All memory requests are processed through path 14 successively. Accordingly, Shiozaki does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths.

Payson is directed to a crossbar switch fabric that includes an arbiter for synchronization purposes. Specifically, in figure 4, Payson teaches arbiter 470 with an input and output parallel bus 430. A single request is parallelized and transmitted over parallel bus 430 from SERDES RX 282. SERDES RX 282 converts serial data into parallel data that is transmitted over a single parallel bus 430 to arbiter 470. Arbiter 470 then transmits its output over a single parallel bus 430. Therefore, Payson teaches an arbiter with a single request port (input parallel bus 430) and a single processing path (output parallel bus 430). Accordingly, Payson does not disclose, teach, or suggest an arbiter that assigns memory requests to first and second processing paths.

Furthermore, Payson does not disclose, teach, or suggest an arbiter with a plurality of request ports, for which it was relied upon in the Office Action's rejection of claim 1.

It is because applicant includes the feature of "...an arbiter having a plurality of request ports...the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path . . . ," that the arbiter is able to assign a first processing path to a first path controller and a second processing path to a second path controller for concurrent activation of memory banks.

As Nystuen, Shiozaki, and Payson are devoid of an arbiter that assigns memory requests to first and second processing paths as set forth in claim 1, Nystuen, Shiozaki, Payson, and combinations thereof fail to disclose, teach, or suggest each and every feature of claim 1. Accordingly, applicant contends that claim 1 is allowable over the applied references.

Claims 9 and 15, while not identical to claim 1, include features similar to claim 1. Accordingly, applicant contends that claims 9 and 15 are also allowable over the applied references for the reasons set forth above.

Claim 17 is directed to an arbitration method for assigning at least one controller to manage a plurality of memory requests from a plurality of requesters to a memory device having at least one memory bank. Claim 17 includes the following features:

> receiving at a plurality of requests ports the plurality of memory requests from the plurality of memory requesters during a current arbitration cycle, each request port configured to receive the memory request from a respective one of the plurality of requesters;
>
> comparing the plurality of memory requesters to a grant history register to identify ones of the plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle;
>
> assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters have not had previous memory requests granted during the current arbitration cycle using fixed priority logic; and
>
> adding the requester of the assigned memory request to the grant history register.

This means that the arbiter looks at a grant history register to determine if a requester has accessed a memory bank during a current arbitration cycle and if that requester has not accessed the memory request, the arbiter may assign the memory request from that requester.

Nystuen fails to disclose, teach, or suggest at least the step of "assigning a memory request to one of the at least one controllers from one of the identified plurality of memory requesters that have not had previous memory requests granted during the current arbitration cycle using fixed priority logic." Nystuen does disclose a history register, i.e., history register 512. The history register in Nystuen, however, is used to determine when to precharge a memory bank rather than for purposes of assigning memory requests as called for in claim 1. Thus, Nystuen fails to disclose, teach, or suggest assigning a memory request to one of at least one controller from the plurality of memory requesters not in the grant history register using fixed priority logic. Likewise, Shiozaki and Payson fail to disclose, teach, or suggest this feature. Accordingly, applicant contends that claim 17 is allowable over the applied references and respectfully requests that the rejection of claim 17 be withdrawn.

Claim 21, while not identical to claim 17, includes features similar to claim 17. Accordingly, applicant contends that claim 21 is also allowable over the applied references for at least the reasons set forth above.

Claims 2-6, 8, 10-14, 16, 18, and 22 include all of the features of the independent claim from which they ultimately depend. Thus, claims 2-6, 8, 10-14, 16, 18, and 22 are also allowable over the cited references for at least the reasons set forth above with respect to independent claims 1, 9, 15, 17, and 21. Accordingly, applicant contends that claims 2-6, 8, 10-14, 16, 18, and 22 are likewise allowable and, therefore, respectfully requests that the rejection of these claims be withdrawn.

Applicant acknowledges with appreciation the Examiner's finding that dependent claims 7, 19, and 20 include allowable subject matter and would be allowed if rewritten in independent form. Applicant submits, however, that there is no need to rewrite these claims in order to place them in condition for allowance because these claims are either directly or indirectly dependent on one of claims 1, 9, and 17, which for the reasons discussed above are also in condition for allowance.

In view of the amendments and remarks set forth above, applicant respectfully submits that claims 1-22 are in condition for allowance and early notification to that effect is earnestly solicited.

Respectfully submitted,

RatnerPrestia

Stephen J. Weed, Reg. No. 45,202
Attorney for Applicant

SJW/RAE/kpc

Dated: September 19, 2007

P. O. Box 980
Valley Forge, PA 19482
(610) 407-0700

The Director is hereby authorized to charge or credit Deposit Account No. **18-0350** for any additional fees, or any underpayment or credit for overpayment in connection herewith.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (571-273-8300) on September 19, 2007.

Kathleen P. Carney